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Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): NLOZ 0668 US

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on 9/21/07

Signature: Michael Ure

Typed or printed name: Michael Ure

Application Number	Filed
10/522,085	01/21/2005

First Named Inventor: VAN WEL

Art Unit	Examiner
2188	ELLIS, KEVIN L

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☐ attorney or agent of record. Registration number _____
- ☒ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34: 33,089

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9/21/07
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NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Atty. Docket
VAN WEL	NL02 0668 US
Serial: 10/522,085	Group Art Unit: 2188
Filed: 01/21/2005	Examiner: ELLIS, KEVIN L

METHOD AND APPARATUS FOR ACCESSING MULTIPLE VECTOR ELEMENTS IN PARALLEL

Certificate of Fax/Mailing Under 37 CFR 1.8

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Michael Ure (Name)

9/21/07 (Signature and Date)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE—PRE-APPEAL REVIEW

Sir:

Responsive to the Office Action of 08/06/2007, please amend this application as follows.

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IN THE CLAIMS

1. (Currently amended) Method for transmitting a vector, in a computer system comprising: a processor; a multi-port memory, which is accessible by the processor, ~~characterized in that~~wherein the method comprises the steps of: passing a base memory address to an address configuration means; defining a set of memory addresses by the address configuration means using the base memory address and a configuration instruction for configuring the address configuration means; transmitting the vector to/from the multi-port memory at one time using the set of memory addresses.

2. (Previously presented) Method according to claim 1, wherein: the address configuration means comprises: a plurality of register files being configured by the configuration instruction, and a plurality of address calculation units for calculating the set of memory addresses; the register files being accessible by the address calculation units; the address calculation units being coupled to the multi-port memory.

3. (Previously presented) Method according to claim 1, wherein: the configuration instruction comprises a set of offsets, each offset in combination with the base memory address defining a second memory address.

4. (Currently amended) A computer system comprising: a processor; a multi-port memory, the multi-port memory being accessible by the processor, ~~characterized in that~~wherein the computer system further comprises an address configuration means,

wherein the address configuration means ~~is conceived to~~ defines a set of memory addresses using a base memory address and a configuration instruction for configuring the address configuration means, and wherein the multi-port memory ~~is conceived to~~ uses the set of memory addresses at one time.

5. (Previously presented) A computer system according to claim 4, wherein: the address configuration means comprises: a plurality of register files arranged to be configured by the configuration instruction, and a plurality of address calculation units for calculating the set of memory addresses; the register fils are accessible by the address calculation units; the address calculation units are coupled to the multi-port memory.

6. (Previously presented) A computer system according to claim 4, wherein: the configuration instruction comprises a set of offsets, each offset in combination with the base memory address defining a second memory address.

7. (Previously presented) A computer system according to claim 4 wherein the multi-port memory and the address configuration means are included in a memory system.

8. (Previously presented) A computer program comprising computer program code means for instructing a computer system to perform the steps of the method as claimed in claim 1.

REMARKS

The Office Action of 08/06/2007 has been carefully considered. Reconsideration in view of the present remarks is respectfully requested.

The claims have been amended as to matters of form only.

Claims 1-8 were rejected as being anticipated by Sakakibara. Claims 1, 2, 4, 5, 7 and 8 were rejected as being anticipated by Duboc. These rejections are respectfully traversed.

A feature of the present invention is that a *single base address* is used to define a set of addresses, that set of addresses being used to transmit a data vector to/from a multi-port memory at one time using the set of memory addresses. The feature of using a single base address to define a set of addresses used in this manner may be clearly seen in Fig. 2 of the specification. The base address is supplied on the input AddrIn to multiple different address calculation units (AU) of an Address Configuration Unit (ACU). Each address calculation unit is provided with a register file (RF). The base memory address *supplied in common* to all of the address calculation units is modified by each of the address calculation units individually using information from each address calculation unit's register file to obtain a set of addresses (Addr) that is applied to the multi-port memory (MEM).

Sakakibara, on the other hand, clearly shows in Figs. 1 and 5 that separate base addresses are used for each memory module. Note the base address register 191-1 of Fig. 5, which is replicated four times in Fig. 1 (RQ0, RQ1, RQ2 and RQ3).

In Duboc, there is no base address per se. Rather, each of a plurality of Data Address Generators (Fig. 2, DAG) is provided with a set of indirect address registers

(Fig. 4). The indirect address registers are programmed independently for each DAG. For each DAG, one of the indirect address registers is selected in order to access memory.

The rejection states: "While the systems of Sakakibara and Duboc have multiple base address registers, nothing prevents these systems from loading the same base address value into teach of the base address registers. This would then mean that a single base address is used to define a set of address as argued by Applicant."

There is no base address in Duboc, only indirect addresses. More importantly, speculation as to how a system *might* be programmed or *might* operate is not a sufficient basis for a rejection.

Accordingly, it may be seen that Sakakibara and Duboc both fail to anticipate the present invention.

Withdrawal of the rejections and allowance of claims 1-8 is respectfully requested.

Respectfully submitted,

Michael J. Ure, Reg. 33,089

Dated: 05/19/2007